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10/612,930	07/07/2003	Shigeyuki Aino	Q76415	6921

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EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,930	AINO ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-22 rejected under 35 U.S.C. 102(b) as being anticipated by Williams et al. (EP 0817053 A1).

In regard to claim 1, Williams et al. disclosed an information processing apparatus comprising:

first and second computer elements (*identical processing sets, fig. 1, 10, 11, 12)* which execute the same instructions substantially simultaneously in substantial synchronism (*operate in synchronism under a common clock, col. 1 lines 10-16)*, and which have first and second memory elements (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20)*, respectively;

a monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* which finds which of said computer elements is out of said synchronism (*output differ, col. 1 lines 34-48)*;

a copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* which copies a part of the data (*copy corresponding memory portion, col. 6 lines 1-6)* stored in said second memory element (*running processor, col. 6 lines 1-6)* to said first memory element (*out-of-sync processor, col. 6 lines 1-6)* when said monitor element (*fault detector unit voter, fig. 1, 17, col. 1*

lines 27-37) finds that said first computer element is out of said synchronism (*output differ, col. 1 lines 34-48)*; and

a third memory element (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18, write buffer for secondary dirty page record, col. 10 lines 29-32)* which stores information (*page of memory that have been dirtied, col. 8 lines 5-18)* to designate which part of the data stored in said second memory element (*running processor, col. 6 lines 1-6)* is copied (*compare records and deduce which pages were actually dirtied in sync, col. 9 lines 47-56)* by said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* when said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48).*

In regard to claim 2, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* is activated (*less traumatic out-of-sync events, col. 2 lines 20-23)* unless a permanent failure (*failure of a single processing set, col. 2 lines 10-19)* occurred in said first computer element (*out-of-sync processor, col. 6 lines 1-6).*

In regard to claim 3, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48)* based on the time in which it receives first

signals from all of said computer modules (*identical processing sets, fig. 1, 10, 11, 12).*

In regard to claim 4, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48)* based on the time (*identical output, col. 1 lines 26-37)*, commands (*commands from the processing sets, fig. 1, 10, 11, 12, col. 1 lines 26-37)* and addresses of requests (*address decoder, fig. 9, 91, col. 11 lines 16-28)* from all of said computer modules (*identical processing sets, fig. 1, 10, 11, 12).*

In regard to claim 5, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information includes an address or addresses (*FIFO buffer, fig. 9, 90, col. 11 lines 16-28)* relating to said first (*out-of-sync processor, col. 6 lines 1-6)* and second memory element (*running processor, col. 6 lines 1-6).*

In regard to claim 6, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information includes an address or addresses (*FIFO buffer, fig. 9, 90, col. 11 lines 16-28)* of access requests (*address decoder enabled in response to the out-of-sync enable signal, fig. 9, 90, 91, 58, col. 11 lines 16-28)* since said monitoring element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds said first computer elements (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48).*

In regard to claim 7, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information includes information relates to data of said computer element being out of said synchronism (*out-of-sync processor, col. 6 lines 1-6)* and has possibility to differ from the corresponding data (*output differ, col. 1 lines 34-48)* of said computer element (*running processor, col. 6 lines 1-6)* being in said synchronism.

In regard to claim 8, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18, write buffer for secondary dirty page record, col. 10 lines 29-32)* includes an address or addresses which is directed by the access request in which said first computer element (*out-of-sync processor, col. 6 lines 1-6)* being out of said synchronism is detected (*output differ, col. 1 lines 34-48)* and by the write access request or the write access requests afterwards by said second computer elements (*running processor, col. 6 lines 1-6).*

In regard to claim 9, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18)* includes an address or addresses when contents of a cache *(write buffer for secondary dirty page record, col. 10 lines 29-32)* is written to said memory element (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20).*

In regard to claim 10, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18)*

indicates the location in said first memory (*out-of-sync processor, col. 6 lines 1-6)* which has possibility of inconsistency (*pages have been modified by the out-of-sync processor, col. 8 lines 5-18)* with said second memory (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20).*

In regard to claim 11, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* copies said part of the data (*copy corresponding memory portion, col. 6 lines 1-6)* by utilizing a direct memory transmission (*copying contents of main memory from running system to out-of-sync processing sets, col. 2 lines 27-48).*

In regard to claim 12, Williams et al. disclosed an information processing apparatus comprising:

first and second computer elements (*identical processing sets, fig. 1, 10, 11, 12)* which execute the same instructions substantially simultaneously in substantial synchronism (*operate in synchronism under a common clock, col. 1 lines 10-16)*, which have first and second memory elements (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20)*, respectively, and each of which has at least one processor (*processor, fig. 3, 20)* and a bus (*internal bus, fig. 3, 23)* connected to said processor;

a monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* which is connected to said bus (*internal bus, fig. 3, 23)* and which finds which of said computer elements is out of said synchronism (*output differ, col. 1 lines 34-48)*;

a copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* which copies a part of the data (*copy corresponding memory portion, col. 6 lines 1-6)* stored in said second memory element (*running processor, col. 6 lines 1-6)* to said first memory element (*out-of-sync processor, col. 6 lines 1-6)* when said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)*is out of said synchronism (*output differ, col. 1 lines 34-48)*; and

a third memory element (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18, write buffer for secondary dirty page record, col. 10 lines 29-32)* which stores information (*page of memory that have been dirtied, col. 8 lines 5-18)* to designate which part of the data stored in said second computer element (*running processor, col. 6 lines 1-6)* is copied (*compare records and deduce which pages were actually dirtied in sync, col. 9 lines 47-56)* by said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* when said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48).*

In regard to claim 13, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* is activated (*less traumatic out-of-sync events, col. 2 lines 20-23)* unless a permanent failure (*failure of a single processing set, col. 2 lines 10-19)* occurred in said first computer element (*out-of-sync processor, col. 6 lines 1-6).*

In regard to claim 14, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48)* based on the time in which it receives first signals from all of said computer modules (*identical processing sets, fig. 1, 10, 11, 12).*

In regard to claim 15, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48)* based on the time (*identical output, col. 1 lines 26-37)*, commands (*commands from the processing sets, fig. 1, 10, 11, 12, col. 1 lines 26-37)* and addresses of requests (*address decoder, fig. 9, 91, col. 11 lines 16-28)* from all of said computer modules (*identical processing sets, fig. 1, 10, 11, 12).*

In regard to claim 16, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information includes an address or addresses (*FIFO buffer, fig. 9, 90, col. 11 lines 16-28)* relating to said first (*out-of-sync processor, col. 6 lines 1-6)* and second memory element (*running processor, col. 6 lines 1-6).*

In regard to claim 17, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information includes an address or addresses (*FIFO buffer, fig. 9, 90, col. 11 lines 16-28)* of access requests (*address decoder enabled in response to the out-of-*

sync enable signal, fig. 9, 90, 91, 58, col. 11 lines 16-28) since said monitoring element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds said first computer elements (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48).*

In regard to claim 18, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information includes information relates to data of said computer element being out of said synchronism (*out-of-sync processor, col. 6 lines 1-6)* and has possibility to differ from the corresponding data (*output differ, col. 1 lines 34-48)* of said computer element (*running processor, col. 6 lines 1-6)* being in said synchronism.

In regard to claim 19, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18, write buffer for secondary dirty page record, col. 10 lines 29-32)* includes an address or addresses which is directed by the access request in which said first computer element (*out-of-sync processor, col. 6 lines 1-6)* being out of said synchronism is detected (*output differ, col. 1 lines 34-48)* and by the write access request or the write access requests afterwards by said second computer elements (*running processor, col. 6 lines 1-6).*

In regard to claim 20, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18)* includes an address or addresses when contents of a cache *(write buffer for secondary dirty page record, col. 10 lines 29-32)* is written to said memory element (*internal state storage memory,*

fig. 2, 22, col. 1 lines 16-20).

In regard to claim 21, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said information (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18)* indicates the location in said first memory (*out-of-sync processor, col. 6 lines 1-6)* which has possibility of inconsistency (*pages have been modified by the out-of-sync processor, col. 8 lines 5-18)* with said second memory (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20).*

In regard to claim 22, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* copies said part of the data (*copy corresponding memory portion, col. 6 lines 1-6)* by utilizing a direct memory transmission (*copying contents of main memory from running system to out-of-sync processing sets, col. 2 lines 27-48).*

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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